ABSTRACT:

The invention relates to an arrangement for testing an integrated circuit (1; 21). In order in this case to avoid a test vector memory and an on-board test system, a data word generator (2; 22), which supplies deterministic data words, means (3, 4, 5, 6; 22, 23, 24, 25, 26, 27) for test pattern generation, which modify the deterministic data words such that prescribed test patterns are produced which can be fed to inputs of an integrated circuit (1; 21) to be tested, and comparison means (12; 30) for comparing test output patterns of the integrated circuit (1; 21) with desired output patterns [lacuna].

Fig. 1